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FOUNDATIONS OF STOCHASTIC COMPUTING SYSTEMS

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During recent years considerable interest has arisen in the possibility of using random variables to represent quantities in a computer[1,2,3]. This is an inefficient means of coding data but enables extremely simple digital hardware to be used to perform complex arithmetic functions. Stochastic computers, as systems using these representations are called, are capable of performing all the operations of the analog computer, addition, subtraction, multiplication, integration, and so on, using simple configurations of digital gates which are readily fabricated using LSI.

Stochastic computing hardware has proved to be an attractive means of realizing advanced adaptive controllers, such as learning machines, and pre-processors for visual pattern-recognition. It is, however, virtually unexplored compared with conventional computing techniques, and no large-scale evaluation of stochastic computing systems has yet taken place. This paper outlines a complete set of arithmetic elements for one form of stochastic computer and discusses their performance.

Stochastic Computing Elements

Information is carried in the stochastic computer by sequences of binary logic levels which change their state only at a clock pulse, and thus may be represented as sequences of 1's and 0's. These sequences do not have a deterministic pattern but are generated by random processes, and defined only by the probability that the logic level will be 1 (or ON) at a clock pulse. This probability, the generating probability of the sequence, is used to represent a quantity in the computer. The range of variation of a probability is from zero through unity, and computational variables have to be coded into this range. Many codings are possible but we will consider only one which gives the same range of variation as in a conventional analog computer.

Let E be a quantity in the range: $-V \leq E \leq V$, which is to be represented by a random binary sequence generated with probability p. A suitable mapping is:-

$$p = (E + V)/2V \qquad (1)$$

and hence -

$$E = (2p-1)V \qquad (2).$$

Maximum positive quantity is represented by a logic level always ON (the sequence - 1111111...); maximum negative quantity by a logic level always OFF (00000000.....); and zero quantity by a logic level randomly ON or OFF with equal probability of either (a sample sequence might be 00010011000101 00000101011...).

Inversion The simple invertor whose output is the complement of its input serves to multiply quantities by -1 (form the negative) in the stochastic computer. If the probability that its input is ON is p, and that its output is ON is p*, then:-

$$p^* = 1 - p \qquad (3).$$

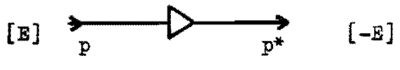
Hence if, from Equation (1), -

$$p = (E+V)/2V \qquad (4)$$

$$p^* = (E^*+V)/2V \qquad (5)$$

then

$$E^* = -E .$$



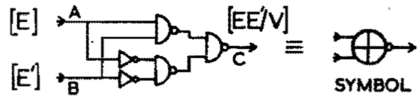
Multiplication An inverted exclusive-OR gates, whose output is ON when its inputs are equal, acts as a four-quadrant multiplier in the stochastic computer. If the probabilities that its inputs are ON are p and p', and the probability that its output is ON is p*, then:

$$p^* = pp' + (1-p)(1-p') \qquad (6)$$

and hence

$$E^* = EE'/V \qquad (7),$$

which is normalized multiplication of E by E'.



$C = A.B \vee \bar{A}.\bar{B}$

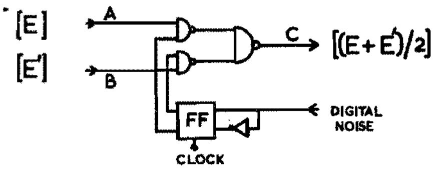
Summation Addition of the quantities represented on a number of lines within the stochastic computer is effected by an element whose output is switched at random to one of these lines. The figure shows a two-input summer in which the output, C, is switched, at a clock pulse, to either line A or line B with equal probability. With the same notation for input and output probabilities as above, we have:

$$p^* = p/2 + p'/2 \qquad (8)$$

and hence

$$E^* = (E + E')/2 \qquad (9),$$

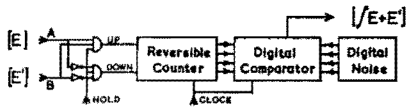
which is normalized summation of E and E'. Through the use of invertors summers may be used as subtractors.



Integration A two-input summing integrator is realized in the stochastic computer by a bi-directional counter which increments by unity when both inputs are ON, and decrements by unity when both inputs are OFF. If the counter has N+1 states, then the value of the integral when it is in its k'th state is:

$$\int = (2k/N - 1)V \qquad (10).$$

In order to give the counter a stochastic output representing the integral, its count is compared at a clock pulse with a random number evenly distributed over the range of the counter.



An important configuration is the integrator in which one of the inputs is fed from the inverted output (unity negative feedback). It may be shown that the fractional count in the counter tends to an unbiased estimate of the probability that the other input will be ON, and hence this configuration acts as a probability to parallel-binary convertor or output device. Similar comparator-based elements may be used as input devices, converting analog or digital variables to probabilities.

Summary This paper serves only as a brief introduction to one family of stochastic computing elements - others are described in detail in the literature, as are applications to system identification, solution of differential equations and pattern recognition. The defect of the stochastic computer is its inefficient coding which restricts its speed - its advantage is its tremendous simplicity of hardware.

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